AMENDMENT

Amendments to the Claims

A complete listing of the claims follows.

1. (Currently Amended) In a computer system, a method for transferring portions of a memory block comprising the steps of:

(a) providing a first data mover with a first start address corresponding to a first portion of a source memory block;

(b) providing a second data mover with a second start address corresponding to a second portion of the source memory ~~block sized differently from the first portion~~;

(c) generating a boundary window to ensure that the first and second memory portions are available for transfer,

(d) ~~(c)~~ verifying that the first portion and the second portion of the source memory block are available for transfer by checking the boundary window before transferring each of the first memory portion and the second memory portion;

(e) ~~(d)~~ after verification, transferring, by the first data mover, the first portion of the source memory block ~~at a first data rate~~; and

(f) ~~(e)~~ after verification, transferring, by the second data mover, the second portion of the source memory block ~~at a second data rate~~.

2. (Currently Amended) The method of claim 1 wherein the computer system is a fault-tolerant computer system (FTC) further comprising at least two central processing units ~~configuring the first data mover with a first chunk end address corresponding to the first portion of the source memory block~~.

3. (Currently Amended) The method of claim 2 wherein one central processing unit is maintained in an on-line state and the other central processing unit is maintained in an off-line state ~~further comprising generating the first chunk end address~~.

4. (Currently Amended) The method of claim 1 ~~further comprising configuring the first data mover with a first write address corresponding to a first portion of a first target memory block~~ wherein at least one data mover stops transferring all memory blocks in response to a system event.

5. (Currently Amended) The method of claim ~~2~~ 4 ~~wherein transferring of the first portion of the source memory block further comprises stopping when the first start address is equivalent to the first chunk end address~~ further comprising configuring the first data mover with a first chunk end address corresponding to the first portion of the source memory block.

6. (Currently Amended) The method of claim ~~2~~ 5 wherein the system event occurs when the first start address is equivalent to the first chunk end address. ~~the transferring of the first portion of the source memory block further comprises stopping when the first start address is equivalent to a predefined end address.~~

7. (Currently Amended) The method of claim ~~1~~ 5 further comprising configuring the second data mover with a second chunk end address.

8. (Original) The method of claim 7 further comprising generating the second chunk end address.

9. (Original) The method of claim 7 further comprising configuring the second data mover with a second write address corresponding to a second portion of a second target memory block.

10. (Currently Amended) The method of claim 7 wherein the ~~transferring of the second portion of the source memory block further comprises stopping~~ system event occurs when the second start address is equivalent to the second chunk end address.

11. (Currently Amended) The method of claim 7 wherein ~~the transferring of the second portion of the source memory block further comprises stopping~~ the system event occurs when the second start address is equivalent to a predefined end address.

12. (Original) The method of claim 1 further comprising configuring the first data mover as a master data mover and the second data mover as a slave data mover.

13. (Original) The method of claim 12 further comprising communicating, by the master data mover, the first start addresses to the slave data mover.

14. (Currently Amended) The method of claim 4 further comprising the step of performing a memory update using the off-line central processing unit ~~transferring the first portion of the source memory block to the first write address corresponding to the first portion of the first target memory block~~.

15. (Currently Amended) The method of claim 4, wherein the system event is a power failure. ~~10 further comprising transferring the second portion of the source memory block to the second write address corresponding to the second portion of the second target memory block.~~

16. (Previously presented) The method of claim 1 further comprising simultaneously transferring the first portion and the second portion of the source memory block.

17. (Currently Amended) In a computer system, a method for transferring portions of a memory block comprising the steps of:

(a) designating a master data mover;

(b) designating a slave data mover in communication with the master data mover;

(c) transmitting a start address to the master data mover, the start address identifying a first memory portion of a source memory block;

(d) transmitting the start address to the slave data mover to enable the slave data mover to determine a next address, the next address identifying a second memory portion of the source memory block ~~sized differently from the first memory portion~~;

(e) checking a boundary window to ensure that the first and second memory portions are available for transfer;

(f) transmitting a first write address identifying a first memory portion of a target memory block to the master data mover and a second write address identifying a second memory portion sized differently than the first memory portion of the target memory block to the slave data mover;

~~(f) verifying that the first portion and the second portion of the source memory block are available for transfer;~~

(g) after verification, transferring the first memory portion of the source memory block to the first write address identifying the first memory portion of the target memory block ~~at a first data rate~~; and

(h) after verification, transferring the second memory portion of the source memory block to the second write address identifying the second memory portion of the target memory block ~~at a second data rate~~.

18. (Canceled)

19. (Canceled)

20. (Previously presented) A system to transfer portions of a memory block comprising:

(a) a first data mover;

(b) a second data mover in communication with the first data mover

over a DM communications bus;

(c) a first memory component having a first portion and a second portion sized differently from the first portion and in communication with the first data mover and the second data mover over a first DM-memory bus; and

(d) a second memory component in communication with the first data mover and the second data mover over a second DM-memory bus;

(e) a boundary window to ensure that the first and second memory components are available for transfer,

wherein the first data mover and the second data mover check the boundary window before transferring at least one of the first memory portion and the second memory portion;

wherein the first data mover transfers the first memory portion to the second memory component over the first DM-memory bus at a first data transfer rate after checking the boundary window, and

wherein the second data mover transfers the second memory portion to the second memory component over the second DM-memory bus at a second data transfer rate after checking the boundary window.

21. (Original) The system of claim 20 wherein the first DM-memory bus is a Peripheral Component Interconnect (PCI) bus and the second DM-memory bus is an Accelerated Graphics Port (AGP) bus.

22. (Previously presented) The system of claim 20 wherein the first data mover transfers the first memory portion at a simultaneous time as the second data mover transfers the second memory portion.

23. (Original) The system of claim 20 wherein the first data mover is a first Direct Memory Access (DMA) engine and the second data mover is a second DMA engine.

24. (New) The system of claim 20 wherein the system is incorporated in a fault-tolerant computer (FTC) system.

25. (New) The system of claim 20 wherein the fault tolerant system includes and an on-line central processing unit (CPU) and an off-line central processing unit (CPU).

26. (New) The system of claim 20 wherein at least one data mover stops transferring all memory blocks in response to a system event.

27. (New) The system of claim 20 wherein the system event is a power failure.

28. (New) The system of claim 20 wherein the system event is a brown out.

29. (New) The system of claim 20 wherein the off-line processor is adapted for receiving memory updates.